REMARKS

Claims 2-7, 9-13, 15-18, 20-25, 27-30, and 32-39 are pending in the present application. In the office action mailed November 17, 2003 ("the Office Action"), the Examiner indicated that claims 1-39 were pending in the present application, and that claims 1, 8, 14, 19, 26, and 31 had been withdrawn from consideration. However, claims 1, 8, 14, 19, 26, and 31 were previously *cancelled* by amendment and not simply withdrawn from consideration (*see* Amendment filed March 5, 2003). Thus, only claims 2-7, 9-13, 15-18, 20-25, 27-30, and 32-39 are currently pending. Acknowledgement by the Examiner of the correct pending claims is requested.

In the Office action, claims 2-7, 9-13, 15-18, and 32-39 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,357,621 to Cox ("the Cox patent") in view of U.S. Patent No. 5,129,069 to Helm *et al.* ("the Helm patent"). Claims 20-25 and 27-30 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,252,612 to Jeddeloh ("the Jeddeloh patent") in view of the Cox patent, and further in view of the Helm patent.

In the Response to Arguments section found at page 2 of the Office Action, the Examiner articulates the rationale for maintaining the rejection of the claims under 35 U.S.C. 103(a) as being unpatentable over the Cox patent in view of the Helm patent. The Examiner has argued that the Helm patent teaches memory module controllers that directly access memory requests. The memory access requests are represented by the address signals provided from the CPU to the memory controller module. The address signals are provided, in particular, to the I/O address decode circuit 33 to determine whether the particular memory module is being addressed. From this, the Examiner infers that the memory controller modules receive memory access requests from the CPU and is given access to the memory storage section 31 through the signal lines ACCESS0-ACCESS7. The teachings of the Helm patent combined with the teachings of the Cox patent, both as characterized by the Examiner, renders the claims unpatentable.

As discussed in the response previously filed on August 28, 2003, the Examiner has mischaracterized both the Cox and Helm patents in order to substantiate the rejection of the claims under 35 U.S.C. 103(a). It then appears that based on the Examiner's mischaracterizations, individual elements found in the two references are simply selected and

combined. Now, in addition to those reasons for withdrawing the claim rejections, the Examiner has ignored the fact that the combination of the Cox and Helm patents, even as characterized by the Examiner in the Response to Arguments section of the Office Action, is unworkable. Based on this, it is unlikely that one ordinarily skilled in the art would have been motivated to combine the references. Moreover, again using the Examiner's own characterizations of the Cox and Helm patents, the combined teachings do not teach or suggest the combination of limitations recited by the rejected claims.

For example, the Examiner has characterized the Cox patent as teaching all of the elements of the claims except for memory controllers that directly access memory requests. *See* page 4 of the Office Action. Included in the Cox patent, according to the Examiner, is a bus 19a-c that links the memory modules together. As discussed in previously filed amendments and responses, the bus 19a-c to which the Examiner is referring simply carries only minimal control information between the MCL controllers 22 of each memory module 20. More specifically, the signal lines 19a-c carry a memory controller out (MCOUT) signal, a memory controller clock signal (MCCLK), and a memory controller N signal (MCIN), respectively. As described in the Cox patent, these signals are passed serially from one MCL controller to the next to configure the memory system upon start-up of the computer system. As also previously discussed, the Examiner relies on the Helm patent for teaching receiving memory access request, where the memory access requests are represented by address signals provided by the CPU to the memory controller module. By combining the teachings of the Cox and Helm patents, the Examiner argues that the claims are unpatentable. However, the Examiner has failed to appreciate the fact that it is unlikely that one ordinarily skilled in the art would combine the provision of the memory addresses (i.e., memory access requests, as characterized by the Examiner) by the CPU to the memory controller module described in the Helm patent with the Cox patent in a manner that would result in teaching or suggesting the combination of limitations recited by the rejected claims. The simple reason is that in the Cox patent, the memory addresses are already being provided from the CPU (and through the system DRAM controller 33) directly to the memory blocks 23, 25, 27, 29. Similarly, as shown in Figure 2 of the Helm patent, although a portion of the addresses are provided to the I/O address decode 33, the address signals A2-A19 are also provided directly to the memory storage section 31 as well. That is, the address signals A2-A19 are provided to the memory devices in the Helm patent, just like in the Cox patent. Thus,

modifying the memory system described in the Cox patent so that the MCL controllers receive the address signals and are passed to one another over the bus 19a-c would be redundant to do so. Eliminating the address lines providing the memory addresses to the memory blocks 23, 25, 27, 29 in order to remove the redundancy is unlikely as well, since doing so would render the memory system described in the Cox patent non-functional.

Additionally, one ordinarily skilled in the art would not be motivated to modify any signal lines between the MCL controllers described in the Cox patent to include address signals (i.e., the memory access commands) because the MCL controllers are directed to configuring the memory module at start-up. After configuration is complete, the operation of the memory module 20 is conventional. The MCL controllers 22 do not need to receive any of the address signals since the address and control signals are provided directly to the memory blocks 23, 25, 27, 29 and the memory block control logic 21.

Thus, even if it is assumed that the Examiner's characterization of the address signals in the Helm patent as being analogous to the memory access commands recited in the claims is accurate, the combined teachings of the Cox patent and Helm patent still fail to teach or suggest a memory controller bus coupled between the first and second memory controllers to pass a memory access request from one memory controller to the other, as recited in the claims. More particularly, the bus 19a-c described in the Cox patent is limited to transmitting MCL controller control signals, and would not be modified to include any such address signals since doing so would be contrary to the purpose of including the MCL controller in a memory module in the first place. The Helm patent fails to disclose any type of memory controller bus that is coupled between memory controllers on which memory access requests can be passed between the memory controllers, even if the address signals represent memory access requests. Based on the description in the Helm patent, the memory address decoding circuit is not coupled to any other memory address decoding circuit, nor does the memory address decoding circuit provide memory access requests to another one in response to receiving a memory access request to access a memory location in a memory array accessible by another memory address decoding circuit.

For the foregoing reasons, the claims 4, 10, 16, 35, and 37 are patentable over the Cox patent in view of the Helm patent. Claims 2, 3, and 5-7, which depend from claim 4, claims 9, and 11-13, which depend from claim 10, claims 15, 17, and 18, which depend from claim 16,

claims 32-34 and 36, which depend from claim 35, and claims 38 and 39, which depend from claim 37, are similarly patentable based on their dependency from a respective allowable base claim. Therefore, the rejection of the claims 2-7, 9-13, 15-18, and 32-39 under 35 U.S.C. 103(a) should be withdrawn.

In rejecting claims 20-25 and 27-30 under 35 U.S.C. 103(a), the Examiner has cited the Jeddeloh patent as teaching a computer having all of the limitations except the first memory and the second memory segmented into a plurality of memory sub-arrays, and the first memory controller and the second memory controller coupled to the memory request to receive memory access requests. *See* page 7 of the Office Action. The combination of the Cox patent in view of the Helm patent has been cited by the Examiner as teaching the elements lacking from the Jeddeloh patent. However, as previously discussed, the combination of the teachings of the Cox and Helm patents fails to teach or suggest memory subsystems recited by the pending claims. Consequently, the Cox and Helm patents fail to make up for the deficiency of the Jeddeloh patent. Therefore, the rejection of claims 20-25 and 27-30 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
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